Claims

[c1] An integrated circuit structure comprising:
a first section comprising logical and functional devices; and
at least one layer of interconnections above said first section, wherein said layer of interconnections comprises:
a first insulator layer;
a second insulator layer above said first insulator layer; and
electrical wiring within said first insulator layer and said second insulator layer, wherein said first insulator layer has a lower dielectric constant than that of said second insulator layer.

[c2] The structure in claim 1, wherein said second insulator layer is harder than said first insulator layer.

[c3] The structure in claim 1, wherein said second layer comprises a protection layer that protects said first layer during rework operations performed on overlying layers of interconnections.

[c4] The structure in claim 1, wherein said first insulator layer comprises one of carbon-doped SiO_2, porous SiO_2, silicon carbide based dielectrics, and polymeric dielectrics.

[c5] The structure in claim 1, wherein said second insulator layer comprises one of nitrides, oxides, Si_3N_4, TaN, Ta, and W.

[c6] The structure in claim 1, wherein said electrical wiring comprises damascene copper.

[c7] The structure in claim 1, wherein said first insulator layer, said second insulator layer, and said electrical wiring comprise a single interconnection layer within said structure.

[c8] An integrated circuit structure comprising:
a first section comprising logical and functional devices; and
a plurality of interconnection layers above said first section, wherein each of said interconnection layers comprises:

a first insulator layer;
a second insulator layer above said first insulator layer; and
electrical wiring within said first insulator layer and said second insulator layer, wherein said first insulator layer has a lower dielectric constant than that of said second insulator layer.

[c9] The structure in claim 8, wherein said second insulator layer is harder than said first insulator layer.

[c10] The structure in claim 8, wherein said second layer comprises a protection layer that protects said first layer during rework operations performed on overlying layers of interconnections.

[c11] The structure in claim 8, wherein said first insulator layer comprises one of a carbon-doped SiO_2, porous SiO_2, silicon carbide based dielectrics, and polymeric dielectrics.

[c12] The structure in claim 8, wherein said second insulator layer comprises one of nitrides, oxides, Si_3N_4, TaN, Ta,W.

[c13] The structure in claim 8, wherein said electrical wiring comprises damascene copper.

[c14] The structure in claim 8, wherein each grouping of said first insulator layer, said second insulator layer, and said electrical wiring comprise a single interconnection layer within said structure.

[c15] A method of reworking interconnection layers above logical and functional layers of an integrated circuit structure, wherein said interconnection layers comprise an upper insulator layer above a lower insulator layer and electrical wiring, wherein said lower insulator layer has a lower dielectric constant than that of said upper insulator layer, said method comprising:
removing a first upper insulator of a first interconnection layer of said interconnection layers; and
removing a first electrical wiring and a first lower insulator of said first interconnection layer in a selective removal process that does not affect a

second upper insulator of a second interconnect layer positioned immediately below said first interconnect layer.

[c16] The method in claim 15, wherein said second upper insulator protects a second lower insulator of said second interconnect layer during said process of removing said first electrical wiring and said first lower insulator.

[c17] The method in claim 15, wherein said removing processes completely remove said first interconnection layer and leave said second interconnection layer in tact, wherein said method further comprises forming a replacement interconnect layer in place of said first interconnect layer.

[c18] The method in claim 15, wherein said process of removing said first upper insulator also removes a portion of said first lower insulator and exposes portions of said electrical wiring,
wherein said method further comprises, after said process of removing said first upper
depositing an etch stop layer on partially removed portions of said first lower insulator and on exposed portions of said electrical wiring.

[c19] The method in claim 18, further comprising after said process of depositing said etch stop layer:
removing said metal wiring, thereby leaving said partially removed portions of said first lower insulator and portions of said etch stop layer; and
removing said etch stop layer.

[c20] The method in claim 19, wherein said etch stop layer protects said first lower insulator during said process of removing said metal wiring.